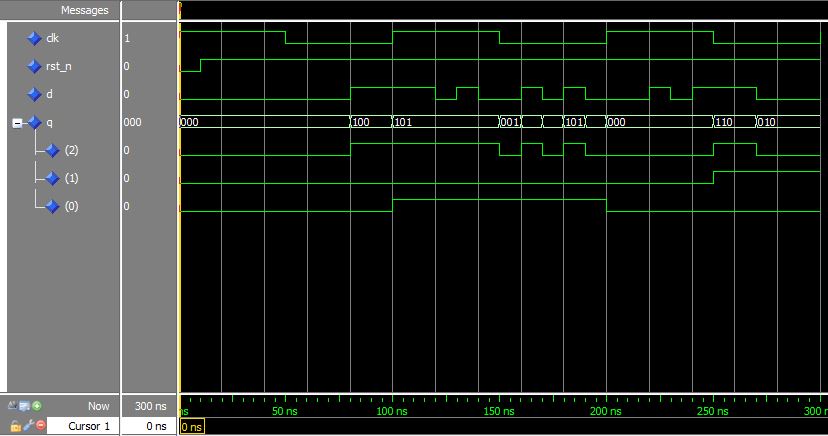
Lab 02: Sequential Logic Modeling

1 Flip-flops and latches

* 1. Different types of Flip-flops/latches
* The types of ff1, ff2, ff3 is D flip-flop.
* Why the sensitive list only contains signals: clk and rst\_n?

For D flip-flop, clock and the reset can trigger changes to the qoutput, but changes ond input will not by itself result in changes to the q output, so the dis not required in the sensitivity list. If add d to the sensitive list, the output is still not changes.

* Result:



* 1. Modeling T flip-flop
* Modelsim: t\_ff.vhd

1. Binary Counter
   1. Behavior description of a binary counter with asynchronous reset and synchronous set

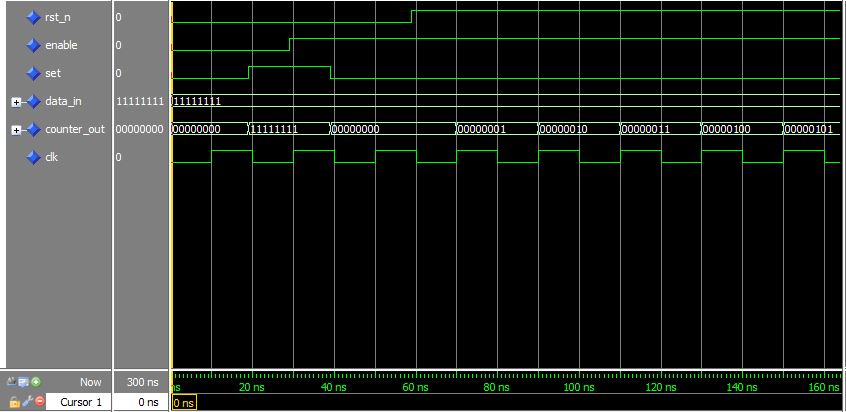
* Modelsim: counter.vhd, counter\_tb.vhd
* What is the important of the rst\_nsignals?

That is asynchronous reset. The advantage of this method is:

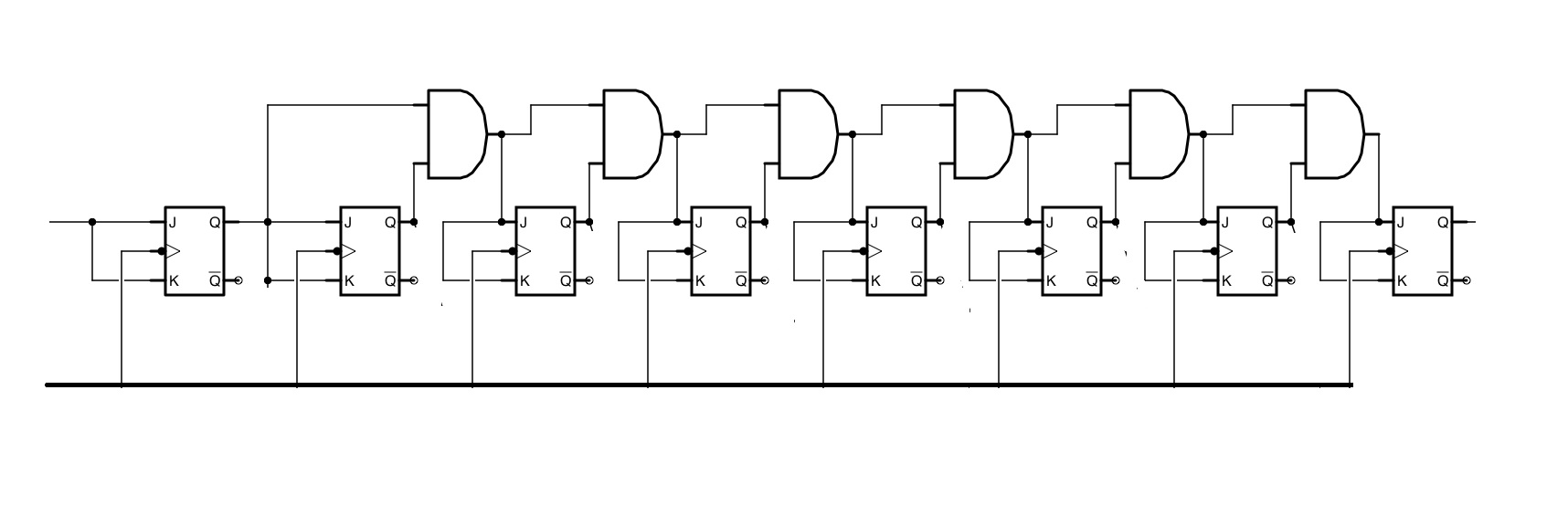
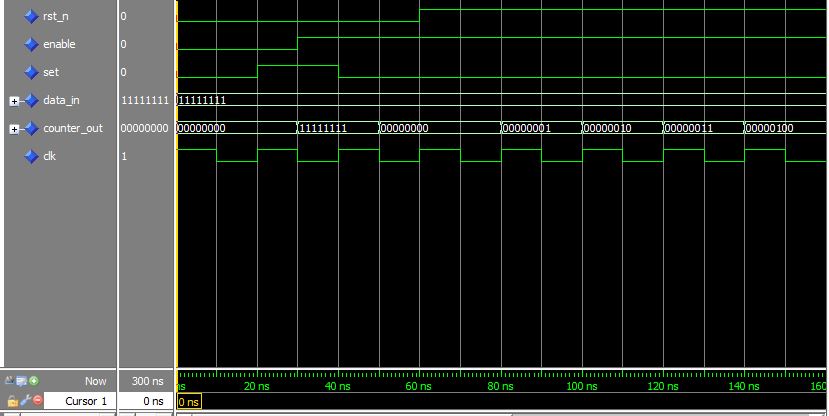
-High speed can be achieved

-Data can be reset without waiting for the clock edge.

* Result:



* 1. Binary counter design using flip-flop
* Modelsim: counter\_tff.vhd, counter\_tff\_tb.vhd, tff.vhd
* Result:



1. Parrallel – to –serial data converter

* Modelsim: converter.vhd, converter\_tb.vhd
* Result:

